

Thermal Enhancement of Systems using Organic Flip-Chip Packages (FC-PBGA) with an Alternate Cooling Path through the Printed Wiring Board

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Abstract

The thermal performance characteristics of organic flip-chip packages (FC-PBGA) incorporating thin (0.5mm), high interconnect density (dense-core) organic substrates has been studied using 1-D calculations and 3-D numerical analysis. Of particular interest is the ability of the substrate to provide an effective thermal path to the printed wiring board (PWB) for high heat dissipation applications. The improvement in thermal impedance of dense core substrates vs. standard core substrates is quantified and shown to be approximately 2x. A package size of 50mm and a chip size of 18mm are assumed for the 3-D analysis. Two types of system boundary conditions, one with a heatsink attached to the top of the package, and one without are considered. For both cases, board-level enhancement is provided with a heatsink or cold plate. Numerical simulations are run to study the effect of the board heatsink on overall heat dissipation. The results indicate that the overall thermal resistance can be reduced by about 43% and that up to 73% or more of the heat dissipated in the chip can be diverted into the board even when a high performance (0.4 C/W) heatsink is used on top of the package. Comparisons are also made with packages with ceramic column grid array packages with similar wiring capability. Results indicate that thin, dense core packages can meet or exceed ceramic package thermal capability for the range of conditions studied here.

Nomenclature

A area
 C_p heat capacity
 k thermal conductivity
 k_{zz} effective out of plane conductivity of substrate
 P Power dissipation (W)
 T Temperature (C)
 T_j Chip temperature (C)
 T_a Air temperature

Symbols

ρ Density
 θ_{ja} Junction-to-ambient thermal resistance (C/W)
 $= (T_j - T_a)/P$

Introduction

Recent developments in chip technology have driven flip-chip substrate improvements for wireability, reliability, electrical and thermal performance. Increasingly, substrates incorporating polymer based (organic) dielectrics have

become popular for many high-end ASIC, and microprocessor applications. They have also generated interest in System-in-package type applications [1].

A new kind of organic substrate for flip chip applications has been developed for next generation chip technologies having a die-pad pitch down to 199 microns [2]-[5]. The 500 micron thick substrate incorporates a 200 micron thick high density core containing 50 micron laser drilled vias on a 200 micron pitch. One or four additional "build-up" layers can be included on either side of the core. These build-up layers are fully customizable as voltage or signal planes. Interconnections within the build-up layers are provided using buried laser drilled vias. Eventually, wiring density requirements will require vertical stacking of buried vias to make better use of available real estate.

Flip-chip package thermal performance has been studied for many years. See references [6]-[12] for a representative sample. More recently, there have been studies investigating the effect of organic substrates on package thermal performance. Calmidi and Sathe [7] studied the effects of package structure on the thermal performance of a flip-chip organic package. Calmidi [4] studied the thermal performance characteristics of a thin, dense core organic flip-chip package. Specific emphasis was placed on the interaction of die size, substrate thermal vias and package structure. No board level enhancement was considered. Ramakrishna and Lee [6] studied the effects of underfill, thermal balls, heat spreader, and overmold on the thermal performance of FC-PBGA packages. The substrate considered was 1.09mm thick and is different from the kind (0.5mm thick) considered here.

This paper reports on the effectiveness of the thermal path through the PWB (or board) for dissipating heat generated in a chip. Although the organic substrate dielectric has poor thermal conductivity which is not helpful for establishing a good thermal path to the PWB, the high density via pattern and a thin substrate profile can potentially, be advantageous. The thermal impedance of this thermal path is first quantified using a one dimensional model calculation and confirmed with three dimensional thermal simulations. Then, the thermal impedance is included in a more detailed three dimensional thermal conduction model that includes the flip-chip package, PWB, critical interfaces, and heatsink boundary conditions. A parametric study of the thermal resistance and heat dissipation characteristics is performed as a function of the board heatsink thermal resistance. Results for the dense

core substrate are compared to those for a ceramic substrate with similar wiring capability.

Thermal Conductivity – Chip to Ball Grid Array (BGA)

Flip Chip packages depend on the thermal path from chip to lid to heat sink as the major approach for power dissipation. With the advent of thin dense core substrates, heat conduction from the flip chip solder joints (C4) to the BGAs at the bottom of the substrate has significantly improved. The thermal resistance from the top substrate pad which joins to the chip solder joint to the bottom substrate pads which joins to the BGA solder joint is shown in Figure 1 as a function of substrate parameters. The units of $\text{mm}^2 \text{C/W}$ are independent of chip area. So, the values in Figure 1 can be divided by the actual area of the chip to yield the thermal resistance in C/W . The substrate of thickness of $50 \mu\text{m}$ thick is assumed. So, the thermal resistance can be scaled linearly to account for actual thickness which ranges from $50 \mu\text{m}$ through $250 \mu\text{m}$ thickness for build-up layers and thin core layers. A $1000 \mu\text{m}$ thickness is representative of the core thickness of a standard core substrate. The key parameters in Figure 1 are via pitch with lower via pitches creating more thermal paths for a given area. The other variables are combinations of hole diameter and thickness which range from $50 \mu\text{m}$ diameter with $12 \mu\text{m}$ thickness ($50\mu\text{mD}/12\mu\text{mT}$) which is typical for build-up vias and thin core plated thru holes (PTHs) up to $200 \mu\text{m}$ hole diameter with $25 \mu\text{m}$ plating thickness which is typical for a standard core. The thermal resistance is additive, thereby a substrate with a $1000\mu\text{m}$ thick core, core via pitch of $600 \mu\text{m}$ and four $50 \mu\text{m}$ thick build-up layers on each side at a $200 \mu\text{m}$ pitch can be derived as:

1. Core thermal resistance from the Figure 1 $200\mu\text{mD}/25\mu\text{mT}$ curve multiplied by 1000 and divided by 50 to normalize for thickness = $3.4 \times 1000 / 50 = 68 \text{ mm}^2 \text{C/W}$.
2. Build-up thermal resistance from the Figure 1 $50\mu\text{mD}/12\mu\text{mT}$ curve multiple by 8 for the 4 build-up layers on each side = $3.6 \times 8 = 28.8 \text{ mm}^2 \text{C/W}$
3. Sum the core plus build-up thermal resistance which results in a total thermal resistance for the standard core = $68 + 14.4 = 96.8 \text{ mm}^2 \text{C/W}$.

The above calculation assumes that the vias are all stacked. This assumption is valid for most of the structure except for the offset between the core via and the build up via stack. The flip chip thermal resistance and BGA thermal resistance can then be added to the substrate thermal resistance to get the total thermal resistance from the bottom of the chip to the top of the PWB. Table 1 shows the material properties that have been used for all the calculations and thermal models. Table 2 shows the geometries used for the calculations. Table 3 shows the calculated thermal resistance of C4, BGA, CCGA and thermal resistance from the top to bottom of the various substrates. Table 4 integrates the solder joint thermal resistances with the substrate thermal resistance to give the total thermal resistance from the bottom of the chip to the top of the PWB for standard core, dense core and also for a 6.75mm thickness ceramic substrate which would

have equivalent wiring capacity but is attached to the PWB with a ceramic column grid array (CCGA).

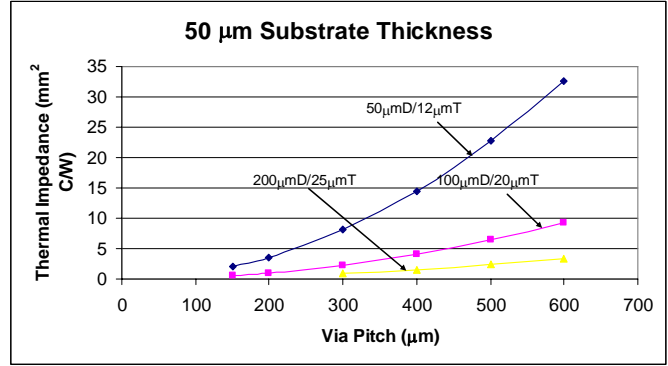


Figure 1 - Substrate Thermal Resistance (C4 to BGA) per Unit Area - $50 \mu\text{m}$ Substrate Thickness

Table 1: Layer thicknesses and material properties

Layer	Thickness (mm)	k(W/m-K)
Lid (above chip)	1	380
Lid-chip interface	0.0635	2
Lid-substrate	0.127	2
Lid-heatsink	0.127	2
Silicon chip	0.74	$k=117.5-0.42*(T-100)$ [7]
Underfill	0.1	0.6
Solder	Variable	47
Laminate dielectric	Variable	0.4
Board dielectric	Variable	0.3
Ceramic substrate	6.75	20

Table 2 - Geometry of Substrate and Solder Elements

Element	Pitch (μm)	Diameter (μm)	Thickness (μm)	Height (μm)
Std Core Core	600	200	25	1000
Dense Core Core	200	50	12	200
Build-up Layer	200	50	12	50
C4 Joint	200	100	NA	100
BGA Joint	1000	780	NA	550
CCGA Joint	1000	510	NA	2210

Table 3 - Thermal Resistivity of Individual Elements

Element	Thermal Impedance ($\text{mm}^2 \text{C/W}$)
C4	10.8
BGA	24.5
CCGA	230
Std Core 4-4-4	96.8
Dense Core 3-4-3	36
Ceramic 6.75 mm	338

Table 4 - Thermal Impedance from Bottom of Chip to Top of PWB

Substrate	Thermal Impedance (mm ² C/W)
Std Core 4-4-4 plus C4 & BGA	132.1
Dense Core 3-4-3 plus C4 & BGA	71.3
Ceramic 6.75 mm plus C4 & CCGA	579

Examining Table 4, there is a major thermal advantage for dense core over standard core and ceramic. In order to determine whether the thermal resistance from the chip to the PWB is valuable it needs to be compared to typical thermal resistances from chip to heat sink. For a 20 mm chip, the chip to heat sink thermal resistance through a 1mm copper lid is about 0.25 C/W (with the lid and interface material properties described later in the paper). With the same chip size (20mm), the dense core thermal resistance from chip to PWB is 0.18 C/W and therefore the thermal path from the chip to the PWB has the potential to provide significant improvement to the total thermal solution.

The next step in the analysis is to look at the thermal situation in a three dimensional manner where the spreading of heat laterally thru the substrate and the PWB as well heatsink boundary conditions are part of the analysis. Even though the vertical thermal impedance of a ceramic substrate high (Table 4), the potential for good spreading with a thick substrate can enhance the thermal effectiveness of the ceramic substrate.

Geometry Description

The following is a description of the substrate, package, PWB, and heatsink used in the numerical study. Figure 2 shows a schematic of the substrate crosssection. It is a “3-4-3” crosssection, indicating four metal layers in the core and three each build-up layers on either side of the core. All metal layers are 12 μm thick. Of the ten metal layers, four layers are signal, and voltage and ground are three each. Voltage and Ground layers are 90% copper, and signal layers are 20% copper. The signal connections are close to the perimeter of the chip to enable wiring. So, the central portion (region A in Figure 3) of the signal layers are customized as voltage or ground. Thus, within region A there are effectively five voltage and ground layers each with direct via connections to voltage and ground C4 connections on the chip. Regions B & C (Figure 3) have four signal layers, and three voltage and ground layers each. The size of region A is dependent on the number of perimeter C4 rows dedicated for signal I/O and the C4 pitch. In this study, the size of region A is 14mm (die size=18mm). The core vias are 50μm in diameter and plating thickness is 12μm. Buried vias in the buildup layer are stacked and assumed to have the same copper crosssection area as the core vias. All vias are on a 200μm pitch within Region A (Figure 3). Within region B, which is the signal escape region and beyond, it is assumed that there are only 1/16 the number of core vias for each C4 bump. So, the core vias are effectively on a 800μm pitch. In region C, which corresponds to the footprint of the lid that

contacts the substrate, core vias are once again on a 200μm pitch. The dielectric material is a particle-filled epoxy dielectric that is suited for laser based processing. The overall thickness of the substrate is 0.5mm. The formed lid (Figure 4) is made of copper and it contacts the top of the chip and substrate. The opening in the lid is 6mm larger than the chip to accommodate the underfill fillet. The thicknesses and thermal conductivity of various materials are shown in Table 1.

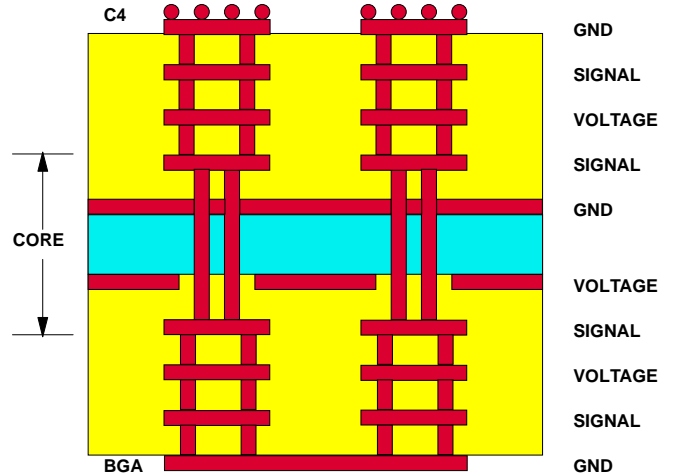


Figure 2: Schematic of substrate crosssection (note: core vias, and buried vias are represented as “stubs”)

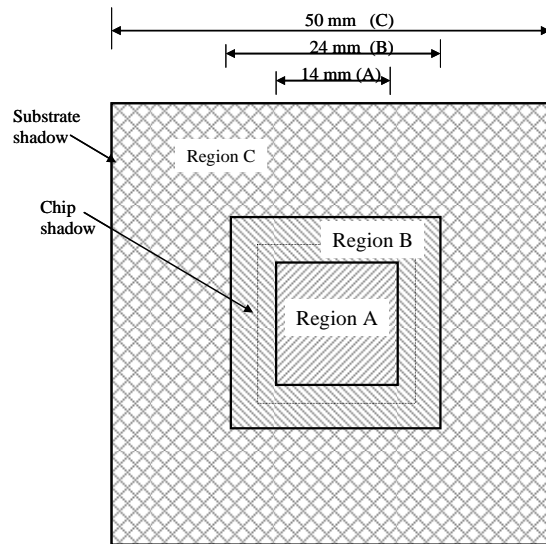


Figure 3: Schematic of the top-side view of the substrate showing via regions under the chip.

Figure 4 shows a schematic of the package assembly that is used in the numerical analysis. The package size is 50mm and the die size is 18mm. The package is attached to a PWB of size 100mm. The overall PWB thickness is 2.3mm. There are nine Voltage/Ground planes that are each 63μm thick. The bottom most layer of the PWB is a ground plane that has clearance holes for voltage and signal via connections only. There are two Aluminum heatsinks of footprint size 50mm, one on top of the package and one on the bottom of the board.

Numerical Procedure

Figure 5 shows a cross-sectional schematic of the model geometry representation. Symmetry is exploited by simulating one quarter of the geometry and applying symmetry boundary conditions. Only heat conduction is simulated with appropriate boundary conditions for the external surfaces. The relevant form of the heat conduction equation in three dimensions is given as,

$$\frac{\partial \rho C_p T}{\partial t} = \nabla^2 (kT) + q''' \quad (1)$$

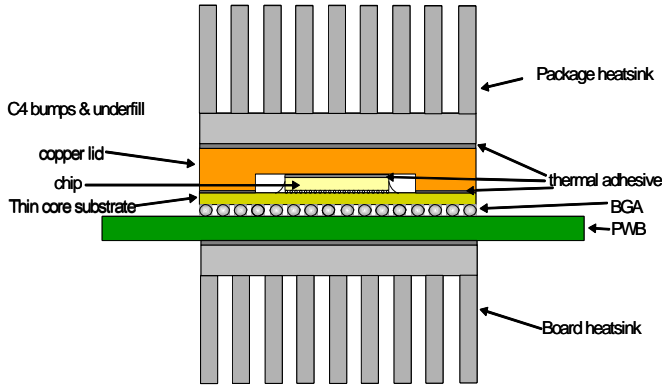


Figure 4: Cross-section of package assembly configuration used in the study

Only steady state situation conditions are simulated. Solid bodies in the geometry are represented as conducting blocks with appropriate thermal conductivities (in some cases orthotropic). Very thin package interfaces are modeled as one dimensional thermal resistance. Only the effects of the heatsink base are included in the model. An effective heat transfer coefficient based on the heatsink thermal resistance is applied to the surface of the heatsink base, as a boundary condition. Material properties and thicknesses are shown in Table 1. Computations were performed using the finite-volume method in the software code Flotherm [13].

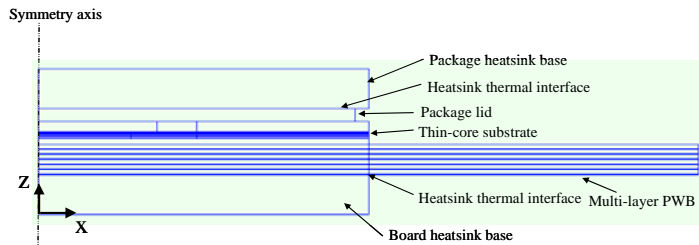


Figure 5: Cross-section of model geometry showing one quarter symmetry

Modeling of high density interconnections: Due to the large number of fine geometric features (vias, clearance holes) within the substrate and the board, it is impractical to include their geometry exactly. Instead, a “micro-macro” approach similar to references [4] and [6] was used. A micromodel is used in a unit cell configuration to predict effective z-direction conductivity (k_{zz}) for the entire unit cell. This computed conductivity is then used as the effective z-direction conductivity of the substrate in the macromodel. Since the substrate has been divided into three regions (Figure 3), three different conductivity values are used based on via

densities in the respective regions. In order to validate the approach and compare it with the 1-D model described earlier (Figure 1), a unit cell with via density and C4 bump density of $250\mu\text{m}$ was constructed. Since the BGA pitch is 1mm ($1000\mu\text{m}$), there are sixteen vias and sixteen C4 bumps for each BGA ball. Figure 6 shows a quarter symmetry model of a thin dense-core substrate with a 3-4-3 cross-section. The core thickness is $200\mu\text{m}$, and each buildup layer is $50\mu\text{m}$ for a total substrate thickness of $500\mu\text{m}$.

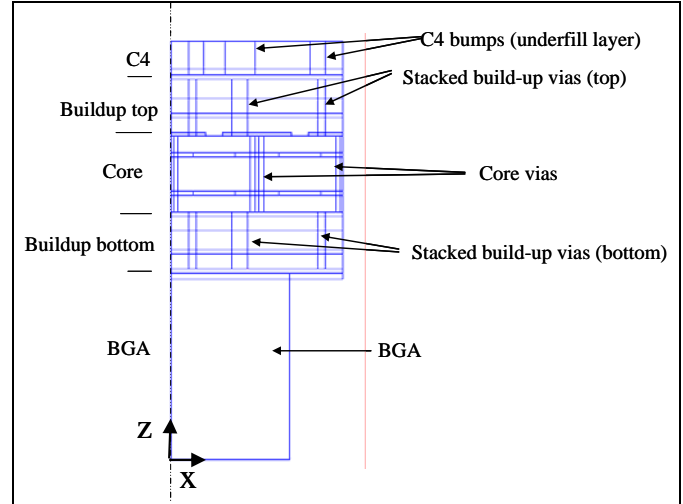


Figure 6: One quarter model geometry of a via unit cell - thin core 3-4-3, $250\mu\text{m}$ via pitch

Table 5: Unit cell impedance (C4-to-BGA) for various configurations.

Name	Impedance ($\text{mm}^2 \text{C/W}$)	1-D (Fig. 1) $\text{mm}^2 \text{C/W}$
Ground BGA 3-4-3	107	106
Voltage BGA 3-4-3	114	106
Ground BGA 1-4-1	91	81
Voltage BGA 1-4-1	100	81

This model was exercised to obtain effective z-direction conductivity by computing the heat flow for a fixed temperature difference across the top and bottom side of the unit cell. Table 5 lists the effective z-direction impedance of the unit cell as obtained from the model. Also listed is a comparison with the 1-D model (Figure 1) for the appropriate geometry. Good agreement is obtained for the 3-4-3 substrate case. Note that even though there are equal numbers of voltage and ground planes, the plane directly above the BGA pad is a ground plane and provides full benefit of z-direction conduction in the vias. As a result there is a small penalty for the voltage BGA z-direction impedance. There is a bigger difference between the 3-D and 1-D calculations for the 1-4-1 substrate because there are fewer metal planes to compensate for the offsetting of the buildup via stack and the core vias. For the full configuration (Figure 5), the estimates from the 1-D calculation were used for the z-axis conductivity in regions

A, B, C. In the x and y axes, the physical planes were included individually with uniform thermal conductivity averaged per the metal area (90% for voltage and ground, 20% for signal)

Validation: The model of the flip-chip package (in Figure 5) used in this study is similar to the experimentally validated one in [4]. However, the boundary conditions are different. The present model was updated with the boundary conditions in [4] and the results obtained were comparable.

Results and Discussion

The model described in the previous section was used to obtain the thermal performance of the assembly. A parametric study was performed by changing the following:

1. Effect of PWB heat sink thermal resistance
2. Effect of substrate type (thin core 3-4-3 and ceramic)
3. Effect of module heat sink (present vs. not present)

An ambient temperature of 25C, and uniform chip heat dissipation (60W when module heatsink is present, and 20W when not present) was assumed. For cases when the module heatsink is used, its thermal resistance value is set at 0.4 C/W. A chip to module heatsink thermal resistance of approximately 0.31 C/W (typical for an 18 mm chip with a high performance thermal interface materials for chip-lid, and lid-heatsink) adds to the module heatsink thermal resistance and gives a total thermal resistance of 0.71 C/W from chip to ambient without accounting for the PWB. As mentioned earlier, a uniform heat transfer coefficient was used to simulate the effect of the heatsink. For example, to simulate a heatsink of thermal resistance 0.4C/W, a heat transfer coefficient of 1000 W/m²-K based on the heatsink area of 2500 mm² is used.

Figure 7 shows the variation of total thermal resistance of the assembly as the thermal resistance of the PWB heat sink is varied. At the lower end, a heatsink thermal resistance of 0.05 C/W representing a cold plate is used. At the higher end a heat sink thermal resistance of 10 C/W representing forced convection cooling (20 W/m²-C and 2500mm² area) without a heatsink is used. This point provides the thermal resistance with little contribution from the thermal path to the PWB. Over the range of values studied, more than 43% improvement in thermal resistance is obtained by effectively utilizing the thermal path to the PWB with a PWB heatsink thermal resistance of 0.05 C/W. The total thermal resistance can be converted to chip power dissipation by fixing the allowable chip temperature rise above the ambient. Figure 8 shows such allowable chip power dissipation for a 60C rise which is typical of many applications. Now more than 73% improvement in allowable power dissipation is obtained as the PWB heatsink thermal resistance improves from 10 C/W to 0.05 C/W. While using a cold plate (0.05 C/W) on the bottom of the PWB may not always be practical, the opportunity to dramatically improve power dissipation capability exists. Even with a PWB heatsink resistance of 0.6C/W, a 30% improvement in power dissipation is obtained. An alternate way of getting an understanding of the board level enhancement is by estimating the thermal

resistance of a single module heatsink that would be needed to yield the same enhancement as two heatsinks, one for the module and one for the PWB. Such an analysis was performed for module and PWB heatsink thermal resistance of 0.4 C/W each. From Figure 7, a total thermal resistance of 0.46 C/W is obtained. Simulations were performed with a PWB heatsink thermal resistance set to 10C/W (representing forced convection without a heatsink). To obtain the same 0.46C/W total resistance, a single module heatsink of 0.21 C/W is required. In some cases where only a module heatsink must be used, the designer is left with no choice but to choose a heatsink of resistance 0.21C/W. In other cases, where there is more design flexibility, it might be advantageous to use two heatsinks of thermal resistance 0.4 C/W each.

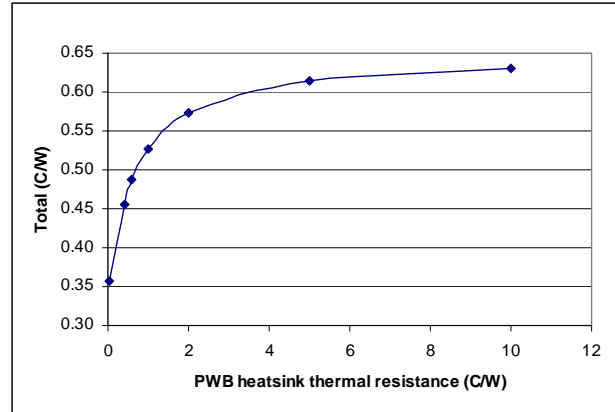


Figure 7: Effect of PWB heatsink thermal resistance on total thermal resistance (thin core 3-4-3 substrate).

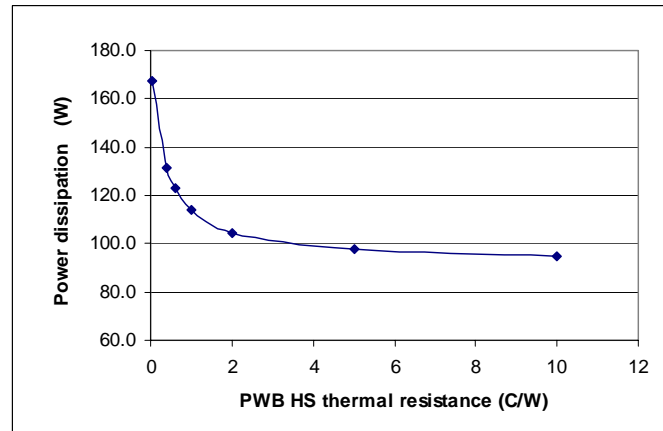


Figure 8: Power dissipation for 60C rise between chip and ambient (thin core 3-4-3 substrate)

Figure 9 shows the effectiveness of the two thermal paths by comparing the heat flow from the chip to the PWB and the module heatsinks. As expected, as the thermal resistance of the PWB heatsink is increased, the percentage of the total heat flowing to it also increases.

Next the effect of a ceramic substrate in the same configuration as the one in Figure 5 is considered. As listed in Table 1, the ceramic substrate thermal conductivity was set at a uniform 20 W/m-K. The substrate thickness is set at 6.75mm. Thin dense-core substrates typically have signal line widths and spaces about 1/3 that of typical ceramic substrates. Thus, in general, three times as many signal layers are

required with typical ceramic substrates. With additional power and ground layers, a total of 27 layers are required. Assuming a layer thickness of $250\mu\text{m}$, the total ceramic substrate thickness is 6.75mm . Figure 10 shows the power dissipation for an allowable chip-ambient temperature rise of 60C for a ceramic substrate. Similar trend is obtained as the one in Figure 8. Comparing the power dissipation values to those for a thin core substrate, an enhancement of between 0.5% and 16.4% is obtained for the thin core substrate. Little or no difference is expected when the PWB heatsink thermal resistance is high since almost all the heat is dissipated through the lid attached to the top of the chip. When the PWB heatsink thermal resistance is low, the improved thermal path of the thin dense core substrate is more significant resulting in a 16.4% improvement vs. ceramic.

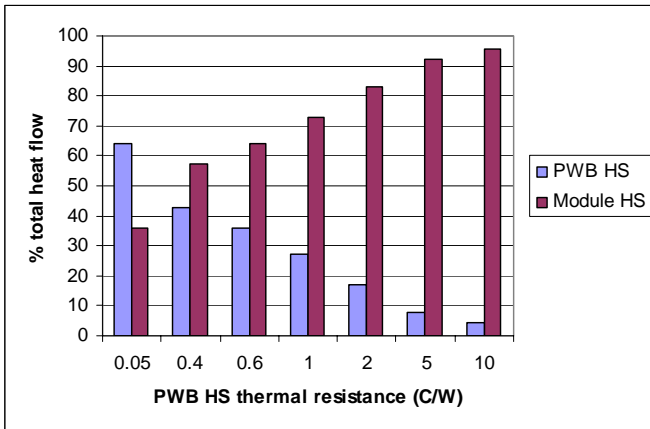


Figure 9: Heat flow from chip to module and PWB heatsinks (thin core 3-4-3 substrate)

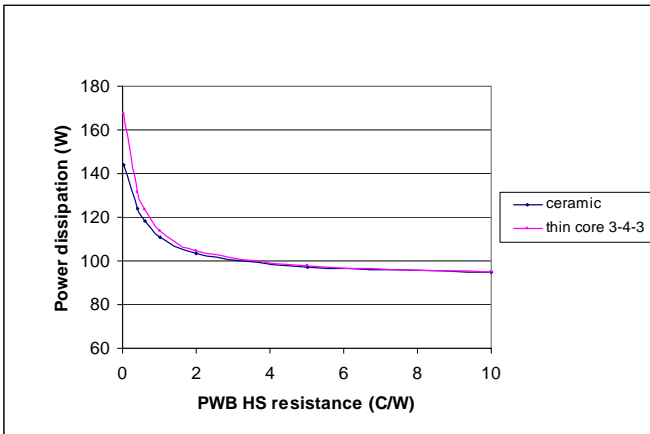


Figure 10: Power dissipation for 60C rise between chip and ambient

In many applications (e.g. space, aerospace), the board is a primary (if not only) means of dissipating heat generated in the chip. The present model is easily adapted to the situation by using a heat transfer coefficient of zero above the module heatsink, essentially insulating the top of the module. When this is done, all of the chip heat is forced to flow into the PWB heatsink. Several cases were simulated under this condition. Figure 11 shows the total thermal resistance variation as a function of the PWB heatsink thermal resistance for both thin dense core and ceramic packages. Unlike the earlier case shown in Figure 7, total thermal resistance varies

almost linearly with the PWB heatsink thermal resistance. In fact, the y-intercept represents the fixed thermal resistance within the assembly. Note that a difference is obtained between the results for the thin dense core substrate and the ceramic substrate, with the thin dense core substrate having lower thermal resistance. The percent improvement for the thin core substrate is amplified as the PWB heatsink thermal resistance is reduced. In Figure 12, the corresponding allowable power dissipation for a 60C temperature rise is shown. In many situations where the board is relied upon for cooling, a cold plate is used as a primary means for dissipating heat generated in the chip. Under the conditions where a cold plate (0.05 C/W) is used for the PWB heatsink, almost 90W can be dissipated when a ceramic substrate is used, and more than 130W can be dissipated when a thin core substrate is used. This represents an almost 50% improvement in power dissipation when a thin dense core substrate is used.

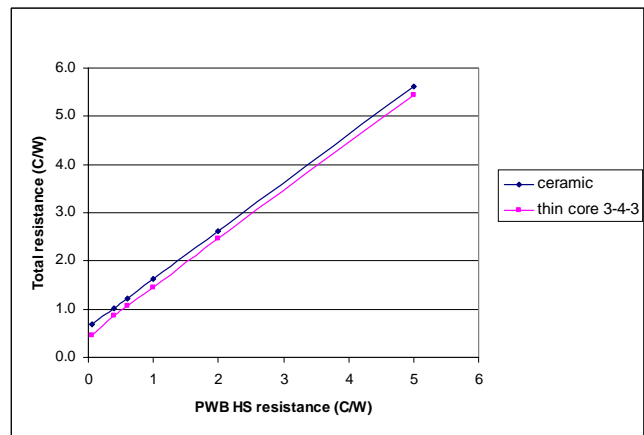


Figure 11: Total thermal resistance as a function of PWB heatsink thermal resistance (no module heatsink)

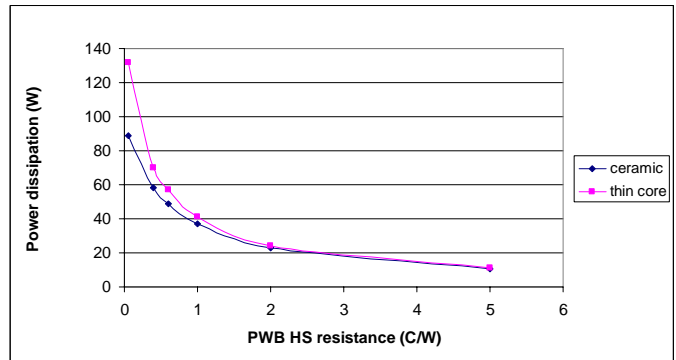


Figure 12: Chip power dissipation for allowable rise of 60C from chip to ambient (no module heatsink)

Summary and Conclusions

The thermal performance of thin dense core organic flip chip package has been studied. Specific focus has been placed on utilizing the substrate to provide an effective thermal path to the PWB. 1-D calculations indicate that the combined effect of the thin profile of the substrate and the large number of high density via interconnections can provide

an effective thermal path to the PWB. A parametric study of a package (50mm module, 18mm die) assembled to a PWB (100mm) with heatsinks (50mm) on both the top of the module and the bottom of the PWB was performed using numerical simulation. The parameters varied were:

1. Effect of PWB heatsink thermal resistance (0.05 C/W to 10 C/W)
2. Effect substrate (thin core 3-4-3 vs. ceramic)
3. Effect of presence of module heatsink (present vs. not present)

The main conclusions of the study are:

When a module heatsink of resistance 0.4 C/W is used,

1. For the thin core substrate, the overall thermal resistance of the assembly decreased by as much as 43%, and the allowable power dissipation for a 60C rise increased by as much as 73%, when compared to the case without a board heatsink. Alternately, a single module heatsink of thermal resistance 0.21 C/W is needed to provide the same thermal resistance as two 0.4 C/W heatsinks each attached to the module and the PWB.
2. For a ceramic substrate of equivalent wireability as the 3-4-3 thin core substrate, the enhancement is similar but lesser in magnitude – as much as 34% decrease in thermal resistance and as much as 52% increase in total power dissipation

When no module heatsink is used,

3. The total thermal resistance increases almost linearly with the PWB heatsink resistance.
4. Enhancement in total power dissipation as much as 50% is obtained by using a thin dense core 3-4-3 substrate over using a ceramic substrate, for an allowable temperature rise of 60C.

From the above, it is clear that thin dense core organic substrates offer considerable opportunity for thermal enhancement of systems by providing an effective, low resistance path to the PWB.

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